Prerequisite: None

Rationale:

Prerequisite: After discussing with the instructors and advisors, it is concluded that a prerequisite is no longer needed because with today's social and educational structure so dependent on computer literacy, the exit goals needed out of the prerequisite are virtually taught in K-12.

Last updated: 11/99

San Bernardino Valley College

Course Outline for ELECTR 265
DIGITAL LOGIC DESIGN

I. CATALOG DESCRIPTION:
Department: Electricity/Electronics
ELECTR 265: Digital Logic Design
3 hours lecture, 3 hours laboratory = 4 Units
Catalog Description: Provides technicians, engineers, and programmers with a working knowledge of digital logic circuits and their application to logic circuits of computers. Includes theory and experience necessary to understand and analyze digital circuits' logic and systems.
Schedule Description: Provides technicians, engineers, and programmers with a working knowledge of digital logic circuits and their application to logic circuits of computers.
Prerequisite/corequisite: None

II. NUMBER OF TIMES COURSE MAY BE TAKEN FOR CREDIT: One

III. EXPECTED OUTCOMES FOR STUDENTS:
Upon completion of this course, students will be able to:
A. Compare and convert number systems from decimal to binary to hexadecimal.
B. Recognize the schematics and use logic gates to arrive at a desired conclusion with any input.
C. Analyze logic circuits by using the sum of products method and Karnaugh maps.
D. Explain the use of flip-flops and registers as applied to logic circuits.
E. Construct various logic circuits and modify circuits to specifications.
F. Explain the operation of various trigger circuits.
G. Analyze waveforms at various points in logic circuits.
H. Troubleshoot digital circuits.

IV. CONTENT:
A. Number Systems
1. Binary number system and number system conversion
2. Octal numbering system
3. Decimal numbering system
4. Hexadecimal numbering system
5. Binary coded decimal (BCD) system
6. Binary addition
7. Binary subtraction
8. Binary 1's complement subtraction
9. Binary 2's complement subtraction
10. Signed 2's complement numbers

B. Logic Gates
   1. Gates
   2. Inverters
   3. OR gates, AND gates, NAND gates, NOR gates
   4. Data control enable/inhibit
   5. AND gate enable/inhibit
   6. OR gate enable/inhibit
   7. NAND gate enable/inhibit
   8. NOR gate enable/inhibit
   9. Summary gate enable/inhibit
   10. NAND as an inverter
   11. NOR as an inverter
   12. Expanding an AND gate
   13. Expanding a NAND gate
   14. Expanding an OR gate
   15. Expanding a NOR gate

C. Waveforms and Boolean Algebra
   1. Waveform analysis
   2. Delayed clock and shift-counter waveforms
   3. Combinational logic
   4. Boolean theorems
   5. DeMorgan's theorems
   6. Designing logic circuits
   7. AND-OR-INVERT gates
   8. Reducing Boolean expressions with Karnaugh

D. Exclusive-OR Gates
   1. Exclusive-OR
   2. Enable/inhibit
   3. Waveform analysis
   4. Exclusive-NOR
   5. Exclusive-OR/NOR
   6. Parity
   7. Even-parity generator
   8. Even/odd-parity generator
   9. Parity checker
   10. Nine-bit parity generator/checker
   11. Comparator

E. Adders
   1. Half adder
   2. Full adder
   3. One's complement adder/subtractor
   4. Two's complement adder/subtractor
   5. Binary-coded-decimal addition
   6. Binary-coded-decimal adder

F. Specifications and Open-Collector Gates
   1. TTL subfamilies
   2. TTL electrical characteristics
   3. TTL supply currents

4. TTL switching characteristics
5. TTL open-collector gates
6. Open-collector applications
7. CMOS
8. CMOS subfamilies
9. CMOS specifications
10. Interfacing TTL to CMOS
11. Emitter coupled logic (ECL)
12. Interfacing ECL to other logic families
13. Surface mount technology

G. Flip-Flops
1. Introduction to flip-flops
2. Crossed NAND set-reset flip-flops
3. Crossed NOR set-reset flip-flops
4. Comparisons
5. Using a set-reset flip-flop as a debounce circuit
6. The gated set-reset flip-flop
7. The transparent D flip-flop
8. The master-slave D flip-flop
9. The pulse edge-triggered D flip-flop

H. Master-Slave D and JK Flip-Flops
1. Toggling a master-slave D flip-flop
2. The JK flip-flop
3. The nonoverlapping clock
4. The shift counter
5. Typical JK ICs

I. Shift Registers
1. Shift register constructed from JK flip-flops
2. Parallel and serial data
3. Parallel-in serial-out
4. Serial data transmission formats
5. IC shift registers
6. Serial data standards
7. The ASCII code

J. Schmitt-Trigger Inputs and Clocks
1. The Schmitt-trigger input
2. Using a Schmitt-trigger to square-up an irregular wave
3. A Schmitt-trigger clock
4. The 555 timer used as a clock
5. Crystal oscillators

K. Digital-to-Analog and Analog-to-Digital Conversions
1. Resistor networks for digital-to-analog conversion
2. The TTL digital-to-analog converter
3. Analog-to-digital conversion using voltage conversion
4. The count-up and compare analog-to-digital converter

L. Decoders, Multiplexers, Demultiplexers and Displays
1. Decoders
2. Demultiplexers

3. Multiplexers
4. Using a multiplexer to reproduce a desired truth table
5. Multiplexer and demultiplexer
6. The 8-trace scope multiplexer
7. The Light Emitting Diode (LED)
8. The 7-segment display
9. The liquid crystal display

V. METHODS OF INSTRUCTION:
Methods of instruction will vary from instructor to instructor but may include:
A. Lecture
B. Discussion between teacher and students plus discussion between individual students

VI. TYPICAL ASSIGNMENTS:
Typical assignments will vary from instructor to instructor but may include:
A. Use a calculator to convert between various numbering systems.
B. Complete variational analyses of a logic diagram circuit.
C. Written homework assigned each week from the questions and problems in each chapter.
Typical Questions:
1. Describe the principles of triggering networks.
2. Draw the truth table for a transparent *D* flip-flop.

VII. EVALUATION(S):
A. Methods of evaluation will vary from instructor to instructor but may include:
1. Quizzes
2. End-of-chapter tests
3. Practical labs with written conclusions graded on content and spelling
4. Final exam
Typical Questions:
a. Write the binary numbers from 100 to 1000.
b. Draw the pinout of a CMOS comparator.
B. Frequency of evaluation will vary from instructor to instructor but may include:
1. Periodic feedback based on chapter quizzes
2. Eight (8) chapter exams
3. Eight (8) practical labs
4. One (1) comprehensive final exam

VIII. TYPICAL TEXT(S):
Bignell, J. W. & Donovan, R. L. Digital Electronics (3^{rd} ed.). ITP Delmar: New York, 1992.

IX. OTHER SUPPLIES REQUIRED OF STUDENTS:
Scientific calculator, scantron answer forms (882 or 882E)